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(54) **MICRODISPLAY WITH REDUCED PIXEL SIZE AND METHOD OF FORMING SAME**

(52) **U.S. Cl.**
CPC ... **G09G 3/3258** (2013.01); **G09G 2300/0465** (2013.01); **H01L 27/3244** (2013.01)

(71) Applicant: **eMagin Corporation**, Hopewell Junction, NY (US)

(72) Inventor: **Ihor WACYK**, Hopewell Junction, NY (US)

(57) **ABSTRACT**

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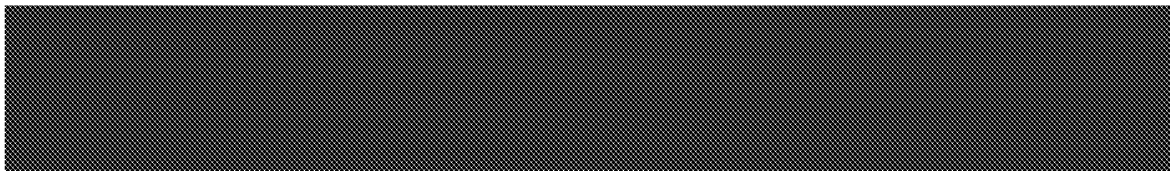
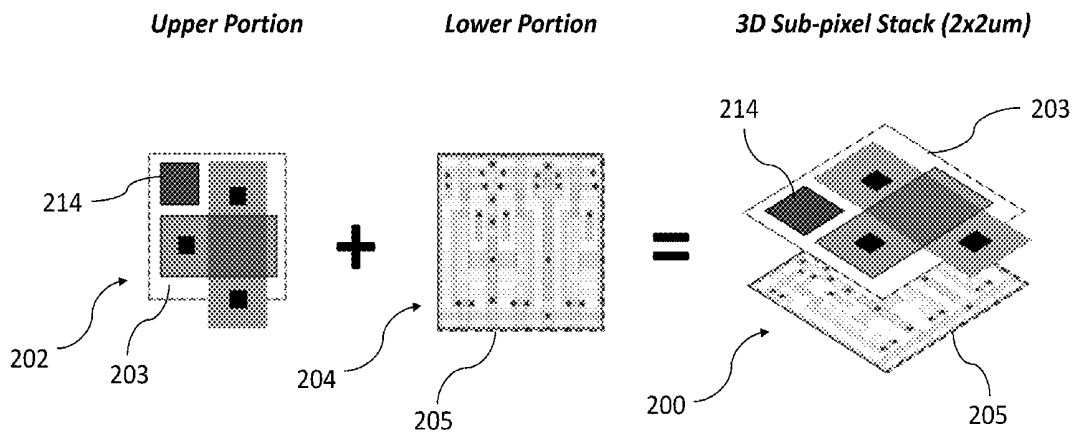
A vertically stacked pixel circuit is provided that includes a high voltage device for driving a pixel on an upper silicon layer, and low voltage circuitry (such as matrix addressing circuitry, data storage circuitry and uniformity compensation circuitry) on a lower silicon layer. The circuitry on the upper and lower silicon layers are electrically connected via a through-silicon via. This unique arrangement allows the high voltage device for driving a pixel to be physically located on top of the larger number of low voltage devices in the lower silicon layer in order to achieve a substantial reduction in overall pixel emission area. The vertically stacked pixel circuit is particularly suited for organic light-emitting diode microdisplays.

Related U.S. Application Data

(60) Provisional application No. 62/632,920, filed on Feb. 20, 2018.

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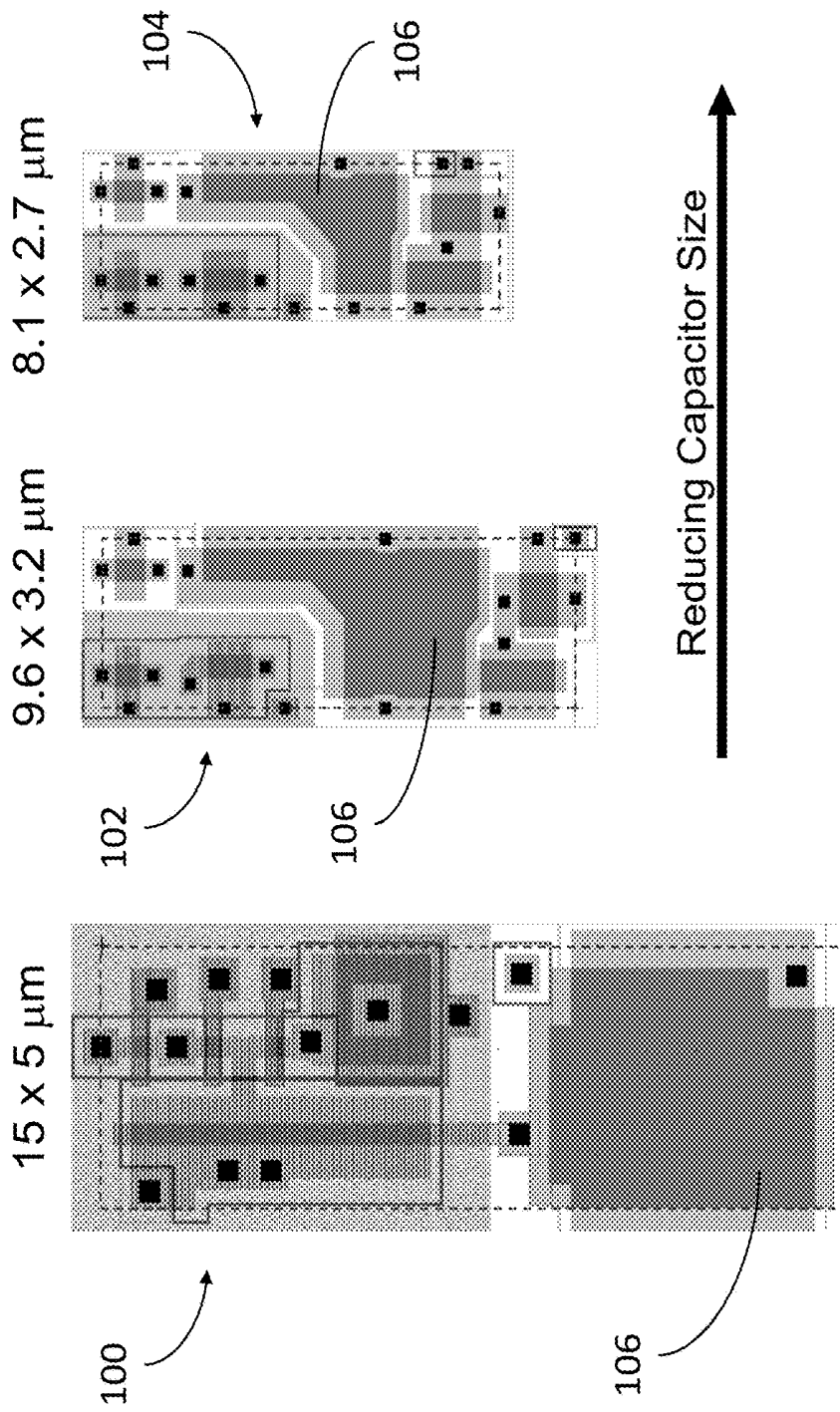


FIG. 1
(Related Art)

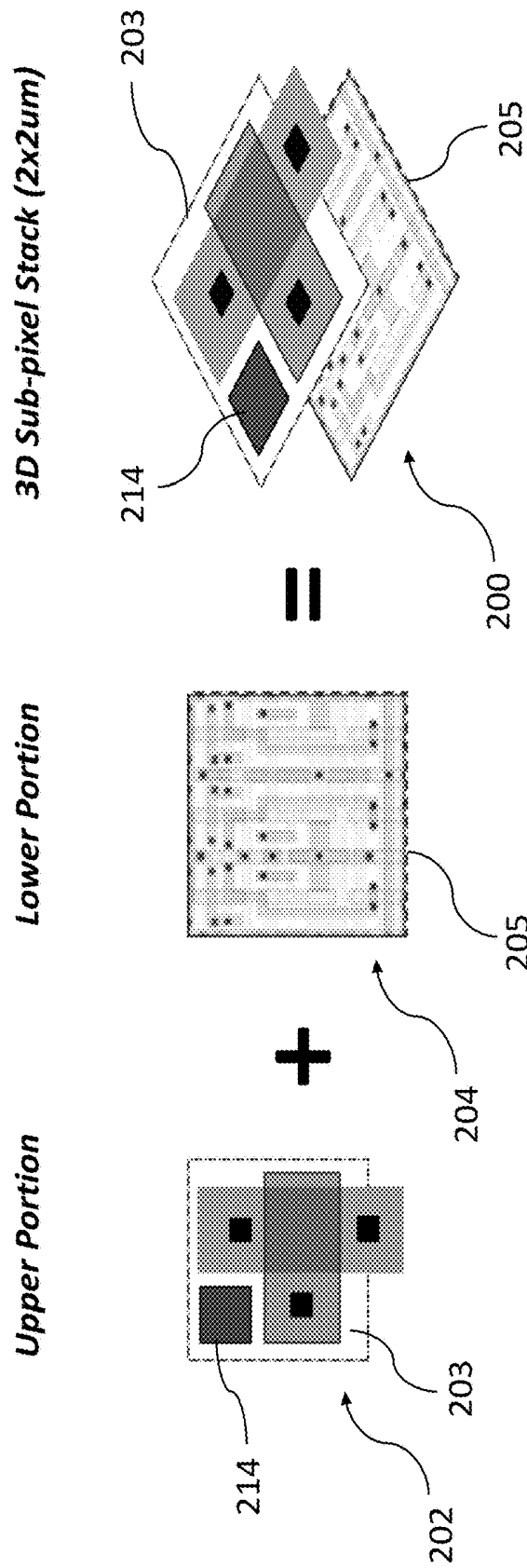


FIG. 2

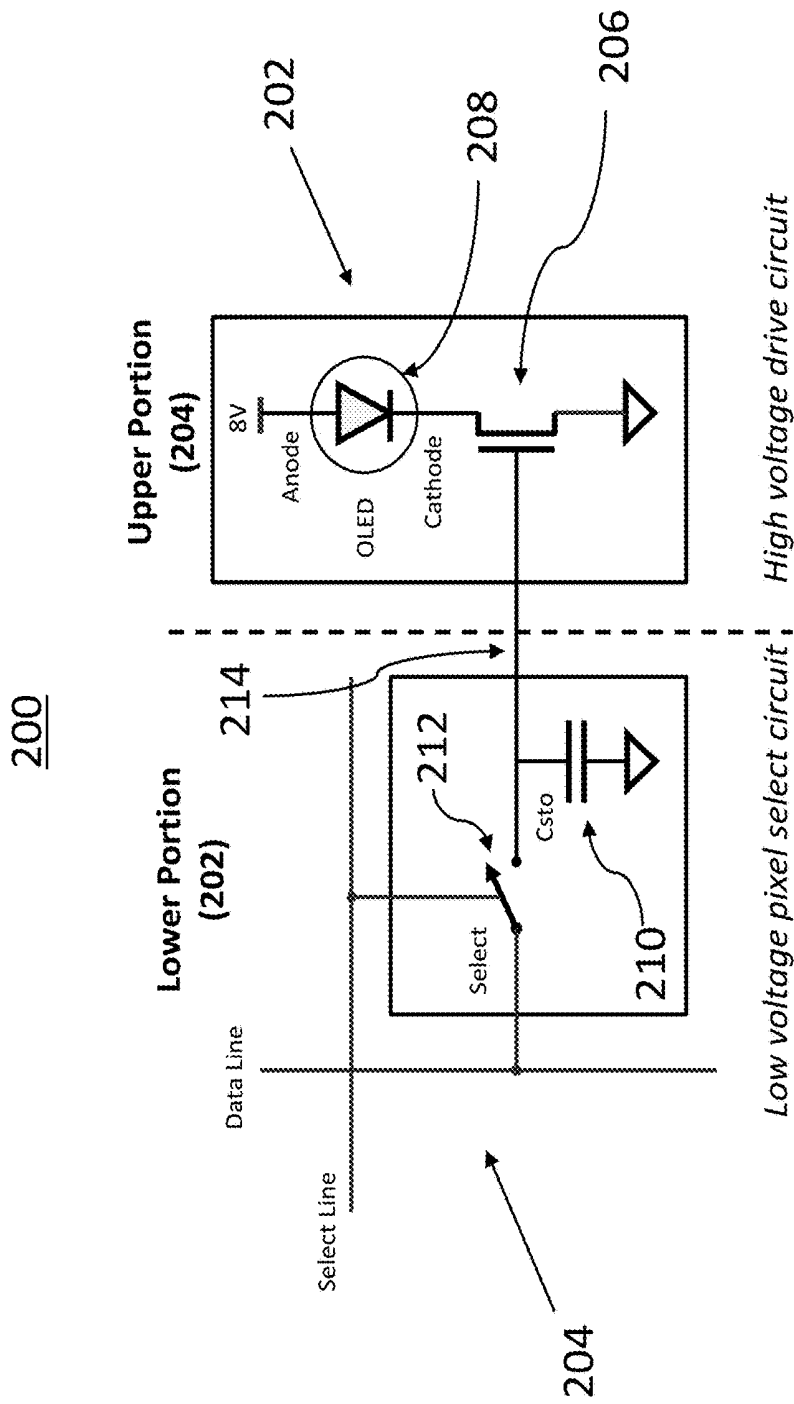


FIG. 3

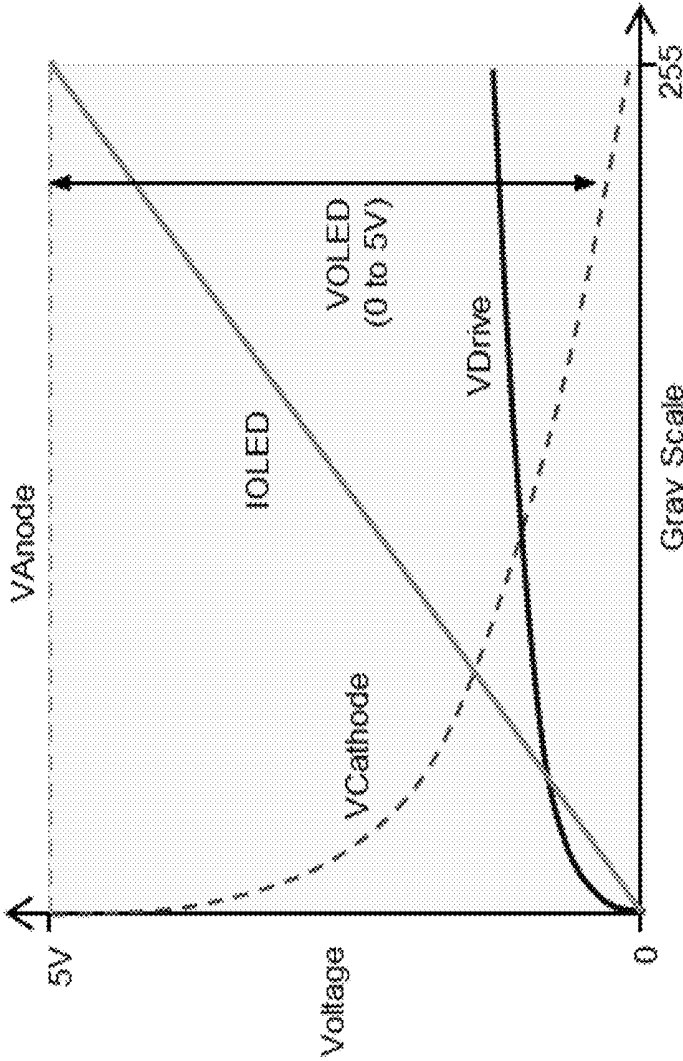


FIG. 4

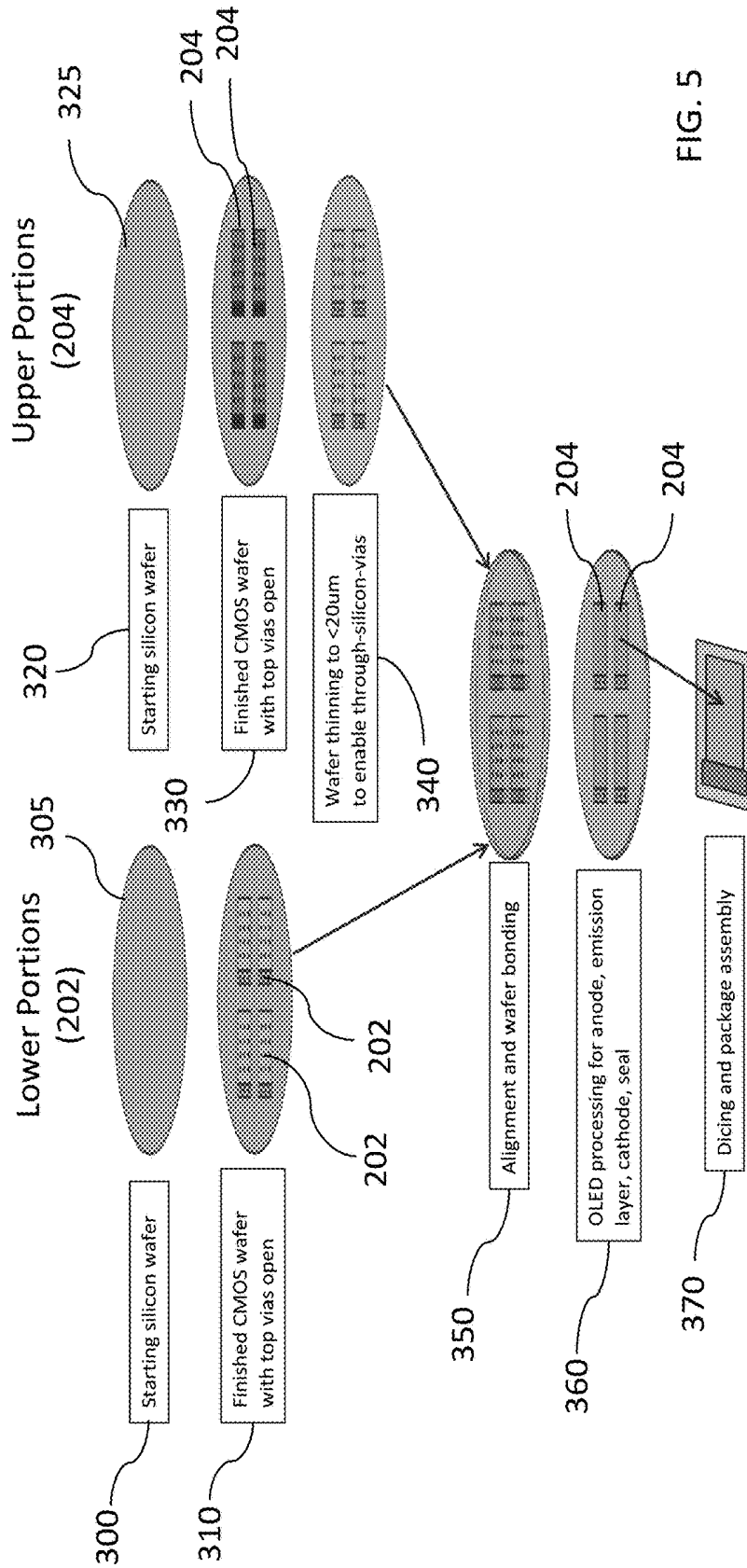


FIG. 5

MICRODISPLAY WITH REDUCED PIXEL SIZE AND METHOD OF FORMING SAME

STATEMENT OF RELATED CASES

[0001] This application claims priority to U.S. Provisional Application Ser. No. 62/632,920, filed Feb. 20, 2018, whose entire disclosure is incorporated herein by reference.

FIELD OF THE INVENTION

[0002] The present invention relates displays in general, and, more particularly, to organic light-emitting diode (OLED) microdisplays with ultra-small pixel sizes.

BACKGROUND OF THE INVENTION

[0003] There is growing interest in building a display with ultra-small pixel sizes for applications such as virtual reality (VR) to improve the user experience. A common problem with existing head-mounted display (HMD) systems is user discomfort after prolonged use due to vergence accommodation conflict (VAC). Among the various solutions proposed to overcome VAC the most comprehensive is expected to be the light field display.

[0004] In the light field approach each pixel comprises multiple sub-pixels, each of which emits directional light. At any particular viewing angle only one (or a very few) of the sub-pixels contributes to the perceived resolution of the image as seen from that direction. As a result the required resolution of a light-field display is increased by the number of directions required for true depth perception.

[0005] In order to achieve adequate directional emission for a particular pixel resolution, a large enough number of sub-pixels must fit into the pixel area, leading to a need for a very small sub-pixel area. In some applications, a sub-pixel area as small as $2\ \mu\text{m} \times 2\ \mu\text{m}$ is required.

[0006] Using conventional silicon backplane technology the minimum sub-pixel area is limited to about $4\ \mu\text{m} \times 4\ \mu\text{m}$ (an area of $16\ \mu\text{m}^2$). This is primarily due to the use of $>5\text{V}$ transistors in the pixel circuit that are needed to operate the OLED. In addition, the capacitor used in the pixel cell for storing the drive level over the duration of the frame cycle can occupy up to 50% of the cell area. Both the pixel transistors and the storage capacitor cannot be shrunk through scaling because the minimum dimensions they require are fixed by the breakdown fields needed to support the $>5\text{V}$ operation.

[0007] As discussed above, a limiting factor in shrinking the OLED pixel circuit is the required area for components that are built on a conventional planar silicon chip. Thus, OLED-based microdisplays having pixels of only a few microns on a side are not achievable using existing planar silicon chip fabrication techniques.

SUMMARY OF THE INVENTION

[0008] An object of the invention is to solve at least the above problems and/or disadvantages and to provide at least the advantages described hereinafter.

[0009] One of the factors that limits the reduction of pixel size for microdisplays is the fact that their components are fabricated using conventional planar silicon chip technology.

[0010] The present invention provides a way around this limitation by constructing the pixel circuits using a three-dimensional (3D) assembly process rather than the two

dimensions used in the planar processing used in standard silicon wafer fabrication. The three-dimensional (3D) pixel circuit of the present invention requires less physical space than conventional pixel circuits. Thus, the present invention enables the fabrication of OLED-based microdisplays with higher pixel densities than prior microdisplays.

[0011] An embodiment of the invention is a vertically stacked circuit, comprising: a lower portion comprising at least one low voltage transistor; and an upper portion, disposed above the lower portion, comprising at least one high voltage transistor; wherein the upper and lower portions are electrically connected via a single electrical connection.

[0012] Another embodiment of the invention is a vertically stacked pixel circuit, comprising: a lower portion comprising at least one low voltage transistor; and an upper portion, disposed above the lower portion, comprising at least one organic light-emitting diode (OLED) and pixel drive circuitry configured to drive the at least one OLED; wherein the upper and lower portions are electrically connected via a single electrical connection.

[0013] Another embodiment of the invention is a method of forming a vertically stacked pixel circuit, comprising: providing a first silicon substrate; forming at least low voltage circuitry and at least one via on the first silicon substrate; providing a second silicon substrate; forming high voltage circuitry and at least one via on the second silicon substrate; attaching the second silicon substrate on top of the first silicon substrate, wherein the at least one via on the second silicon substrate is aligned with the at least one via on the first silicon substrate to form a through-silicon via, and wherein the low voltage circuitry and the high voltage circuitry are electrically connected via the through-silicon via; and fabricating at least one organic light-emitting diode on the second silicon substrate.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements wherein:

[0015] FIG. 1 are schematic drawings of pixel circuits of different sizes formed using a conventional silicon fabrication process;

[0016] FIG. 2 is a schematic drawing of a vertically stacked pixel circuit, in accordance with an illustrative embodiment of the present invention;

[0017] FIG. 3 is a circuit diagram of the vertically stacked pixel circuit of FIG. 2, in accordance with an illustrative embodiment of the present invention;

[0018] FIG. 4 is a graph showing the operating signal values for the pixel circuit of FIGS. 2 and 3, in accordance with an illustrative embodiment of the present invention; and

[0019] FIG. 5 is a flowchart of a fabrication method for an OLED microdisplay that utilizes the pixel circuit of FIGS. 2 and 3, in accordance with an illustrative embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0020] In the following detailed description of various embodiments of the system and method of the present invention, numerous specific details are set forth in order to

provide a thorough understanding of various aspects of one or more embodiments. However, the one or more embodiments may be practiced without some or all of these specific details. In other instances, well-known methods, procedures, and/or components have not been described in detail so as not to unnecessarily obscure aspects of embodiments.

[0021] While preferred embodiments are disclosed, still other embodiments of the system and method of the present invention will become apparent to those skilled in the art from the following detailed description, which shows and describes illustrative embodiments. As will be realized, the following disclosure is capable of modifications in various obvious aspects, all without departing from the spirit and scope of the present invention. Also, the reference or non-reference to a particular embodiment of the invention shall not be interpreted to limit the scope of the present invention.

[0022] FIG. 1 are schematic drawings of pixel circuits 100, 102 and 104 of different size formed using a conventional silicon fabrication process. Each pixel circuit includes five transistors and one capacitor 106. The physical dimensions of pixel circuits 100, 102 and 104 are $15\ \mu\text{m}\times 5\ \mu\text{m}$, $9.6\ \mu\text{m}\times 3.2\ \mu\text{m}$ and $8.1\ \mu\text{m}\times 2.7\ \mu\text{m}$, respectively.

[0023] The progressive reduction in pixel area for pixel circuits 100, 102 and 104 is achieved primarily by reducing the area of the storage capacitor 106. In the $8.1\ \mu\text{m}\times 2.7\ \mu\text{m}$ pixel circuit 104, the size of the storage capacitor 106 is the minimum acceptable value for that size pixel. Additional pixel-size reduction is difficult, if not impossible, using conventional fabrication techniques.

[0024] The present invention enables an OLED microdisplay having pixels that include small sub-pixel areas as small as $2\ \mu\text{m}\times 2\ \mu\text{m}$ (an area of $4\ \mu\text{m}^2$) or smaller. Each pixel in the array includes pixel circuitry and regions of OLED material, where the pixel circuitry and the OLED material are integrated on a substrate via a 3D silicon assembly process.

[0025] A 3D pixel is fabricated so as to be split between a single high voltage device for driving the OLED on an upper silicon layer, and a group of low voltage devices and a trench capacitor that are located on a lower silicon layer. This unique arrangement allows the large high voltage device to be physically located on top of the larger number of low voltage devices in the lower silicon layer in order to achieve a substantial reduction in overall pixel emission area. With this circuit configuration, the lower silicon layer functions can be implemented using advanced silicon technology, such as a DRAM fabrication process, which also has the benefit of allowing a vertical trench capacitor to be used for data storage, thereby further reducing the pixel area dimensions. As used herein, the term "high voltage device" or "high voltage transistor" refers to a device or transistor designed to operate at voltages greater than approximately 3 volts and the term "low voltage device" or "low voltage transistor" refers to a device or transistor that is designed to operate at voltages of approximately 3 volts or lower.

[0026] FIG. 2 is a schematic drawing of a vertically stacked pixel circuit 200 and FIG. 3 is a circuit diagram of the vertically stacked pixel circuit 200, in accordance with an illustrative embodiment of the present invention.

[0027] The pixel circuit 200 includes an upper portion 202 that is fabricated on an upper silicon layer 203 and a lower portion 204 that is fabricated on a lower silicon layer 205. Upper portion 202 includes a high voltage drive transistor 206, suitably a 5 volt drive transistor, and an OLED 208. The

devices that make up portion 202 are preferably fabricated on a thinned silicon wafer, which includes through-silicon via (TSV) 214 at each pixel for enabling an electrical connection to the circuitry of lower portion 204.

[0028] Lower portion 204 is a low voltage pixel-select sub-circuit that is fabricated on a lower silicon layer 205 and includes matrix addressing circuitry, data storage circuitry and uniformity compensation circuitry. The data storage circuitry preferably includes a storage capacitor 210, suitably a trench capacitor. The matrix addressing circuitry preferably includes a selection switch 212, suitably a switching transistor. The uniformity compensation circuitry preferably includes low voltage transistors (not shown) used for generating a local correction signal to the input data to ensure identical brightness performance among pixels despite process or aging related variations in drive transistors 206 and/or OLEDs 208 between different pixels. All of the devices that make up lower portion 204 operate at a lower voltage than the upper portion 202, suitably approximately 1V, and are preferably fabricated using a high-density scaled-silicon process.

[0029] Thus, the pixel circuit 200 is split into a drive transistor 206 (e.g., a 5 volt transistor) at the upper portion 202 and a group of low voltage (e.g., 1 volt) devices at the lower portion 204, with only a single connection point (TSV 214) needed to electrically connect the upper and lower portions 202 and 204 for each pixel. Since the lower portion 204 is operating at a low voltage in this design, it can be readily scaled and the storage capacitor 210 at the lower portion 204 can be built in a very small area using a trench structure commonly used in DRAM chips. The pixel circuit 200 is particularly suited for implementing an OLED microdisplay having pixels that include small sub-pixel areas as small as $2\ \mu\text{m}\times 2\ \mu\text{m}$ (an area of $4\ \mu\text{m}^2$) or smaller, with each sub-pixel implemented with a respective pixel circuit 200.

[0030] FIG. 4 is a graph showing the operating signal values for the pixel circuit 200. "VAnode" denotes the voltage at the anode of side of the OLED, "VCathode" denotes the voltage at the cathode side of the OLED, "IDLED" denotes the current through the OLED, "VOLED" denotes the voltage across the OLED and "VDrive" denotes the voltage applied to the gate of drive transistor 206.

[0031] FIG. 5 is a flowchart of a fabrication method for an OLED microdisplay that utilizes the 3D pixel circuit 200, in accordance with an illustrative embodiment of the present invention. The upper portion 204 and lower portion 202 are fabricated separately using silicone fabrication processes.

[0032] With regards to the lower portion 202, at step 300 a silicon wafer 305 is provided. At step 310, the CMOS devices for multiple lower portions 202 are fabricated on the silicone wafer with top vias open that will enable the TSV 214 in each finished pixel circuit 200.

[0033] With regards to the upper portions 204, at step 320 a silicon wafer 325 is provided. At step 330, the CMOS devices for multiple upper portions 204 are fabricated on the silicone wafer with top vias open that will enable the TSV 214 in each finished pixel circuit 200. At step 340, the silicon wafer is mechanically polished so as to reduce the thickness of the silicon wafer (thinning the silicon wafer) to preferably less than $20\ \mu\text{m}$ in order to enable the TSV 214.

[0034] At step 350, the silicon wafer that contains the lower portions 202 and the silicon wafer that contains the upper portions 204 are aligned and bonded. The silicon wafers are preferably bonded by using a low-temperature

thermo-compression process for bonding ultra-fine pitch cu-to-cu metals used in the TSV 214. Special in-situ alignment cameras known in the art for 3D wafer bonding can be used for wafer alignment. At step 360, the OLEDs are fabricated on the upper portions 204. The OLEDs are fabricated by using evaporation and deposition techniques that are known in the art for fabricating OLEDs. Then, at step 370, the combined wafers are diced to yield multiple OLED display panels that are then assembled into a display package.

[0035] The foregoing embodiments and advantages are merely exemplary, and are not to be construed as limiting the present invention. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. Various changes may be made without departing from the spirit and scope of the invention.

What is claimed is:

1. A vertically stacked circuit, comprising:
 - a lower portion comprising at least one low voltage transistor; and
 - an upper portion, disposed above the lower portion, comprising at least one high voltage transistor;
 - wherein the upper and lower portions are electrically connected via an electrical connection.
2. The circuit of claim 1, wherein the high voltage transistor comprises a transistor designed to operate at a voltage greater than 3 volts.
3. The circuit of claim 1, wherein the lower portion and the upper portion are formed on respective silicon layers.
4. The circuit of claim 3, wherein the electrical connection comprises a through-silicon via.
5. The circuit of claim 1, wherein the upper portion further comprises at least one organic light-emitting diode (OLED).
6. The circuit of claim 1, wherein a length and width of the circuit are less than $4\ \mu\text{m}\times 4\ \mu\text{m}$.
7. A vertically stacked pixel circuit, comprising:
 - a lower portion comprising at least one low voltage transistor; and
 - an upper portion, disposed above the lower portion, comprising at least one organic light-emitting diode (OLED) and pixel drive circuitry configured to drive the at least one OLED;
 - wherein the upper and lower portions are electrically connected via an electrical connection.
8. The pixel circuit of claim 7, wherein the lower portion comprises matrix addressing circuitry, data storage circuitry and uniformity compensation circuitry.
9. The pixel circuit of claim 7, wherein the pixel drive circuitry comprises at least one high voltage transistor.
10. The pixel circuit of claim 8, wherein the matrix addressing circuitry comprises a selection switch and the data storage circuitry comprises a storage capacitor.

11. The pixel circuit of claim 10, wherein the storage capacitor comprises a trench capacitor.

12. The pixel circuit of claim 7, wherein the lower portion and the upper portion are formed on respective silicon layers.

13. The pixel circuit of claim 7, wherein the electrical connection comprises a through-silicon via.

14. A microdisplay comprising a plurality of sub-pixels, wherein each sub-pixel comprises the pixel drive circuit of claim 7.

15. The pixel circuit of claim 12, wherein the silicon layer containing the lower portion and the silicon layer containing the upper portion are bonded together.

16. The pixel circuit of claim 12, wherein a length and width of the pixel circuit are less than $4\ \mu\text{m}\times 4\ \mu\text{m}$.

17. A method of forming a vertically stacked pixel circuit, comprising:

- providing a first silicon substrate;
- forming at least low voltage circuitry and at least one via on the first silicon substrate;
- providing a second silicon substrate;
- forming high voltage circuitry and at least one via on the second silicon substrate;
- attaching the second silicon substrate on top of the first silicon substrate, wherein the at least one via on the second silicon substrate is aligned with the at least one via on the first silicon substrate to form a through-silicon via, and wherein the low voltage circuitry and the high voltage circuitry are electrically connected via the through-silicon via; and
- fabricating at least one organic light-emitting diode on the second silicon substrate.

18. The method of claim 17, wherein the low voltage circuitry comprises matrix addressing circuitry, data drive circuitry and uniformity compensation circuitry.

19. The method of claim 17, wherein the matrix addressing circuitry comprises a selection switch and the data storage circuitry comprises a storage capacitor.

20. The pixel circuit of claim 19, wherein the storage capacitor comprises a trench capacitor.

21. The method of claim 17, wherein the high voltage circuitry comprises pixel drive circuitry.

22. The method of claim 21, wherein the pixel drive circuitry comprises at least one high voltage transistor.

23. The method of claim 17, further comprising thinning the second silicon substrate, prior to attaching the second silicon substrate to the first silicon substrate.

24. The method of claim 23, wherein the second silicon substrate is thinned so that its thickness is less than $20\ \mu\text{m}$.

25. The method of claim 17, further comprising fabricating a microdisplay using a plurality of the vertically stacked pixel circuits.

26. The method of claim 17, wherein a length and width of the pixel circuit are less than $4\ \mu\text{m}\times 4\ \mu\text{m}$.

* * * * *

专利名称(译)	具有减小的像素尺寸的微显示器及其形成方法		
公开(公告)号	US20190259337A1	公开(公告)日	2019-08-22
申请号	US16/279809	申请日	2019-02-19
申请(专利权)人(译)	eMagin公司		
当前申请(专利权)人(译)	eMagin公司		
[标]发明人	WACYK IHOR		
发明人	WACYK, IHOR		
IPC分类号	G09G3/3258 H01L27/32		
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优先权	62/632920 2018-02-20 US		
外部链接	Espacenet USPTO		

摘要(译)

提供垂直堆叠的像素电路，其包括用于驱动上硅层上的像素的高压器件，以及下硅层上的低压电路（诸如矩阵寻址电路，数据存储电路和均匀性补偿电路）。上硅层和下硅层上的电路通过硅通孔电连接。这种独特的布置允许用于驱动像素的高压器件物理地位于下硅层中的较大数量的低压器件的顶部，以实现整个像素发射区域的显著减小。垂直堆叠的像素电路特别适用于有机发光二极管微显示器。

